Retention of High Efficiency Video Coding (HEVC)

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***Abstract*—**This paper holds the information of extensively anamnesis and summery on High efficiency video coding (HEVC). This makes awesome conceivable to give the analytic and prognostic procedures in the latest video standard introduced by ITU-T video coding expert group and ISO/IEC MPEG and which thus help in the field of video processing. The proposed study says that the different algorithm and the architectural requirements for the implementation, which involves the different parallelism, pipelining, FSM and other techniques.

Keywords*—*HEVC; video standards; CABAC; CAVLC; Inter and Intra prediction unit.

I. INTRODUCTION

In order to provide better compression and video quality compared to previous standards, H.265 / MPEG-4 part 10 video coding standard was recently developed by the JVT (Joint Video Team) consisting of experts from VCEG and MPEG. H.265 fulfills Significant coding efficiency, simple syntax specifications, and seamless integration of video coding into all current protocols and multiplex architectures. Thus H.265/mpeg can support various applications like video broadcasting, video streaming, and video conferencing over fixed and wireless networks and over different transport protocols.

H.265/ MPEG-4 part 10 video coding standard has the same basic functional elements as previous standards (MPEG-1, MPEG-2, MPEG-4 part 2, H.261, H.263) , i.e., transform for reduction of spatial correlation, quantization for bit rate control, motion compensated prediction for reduction of temporal correlation, entropy encoding for reduction of statistical correlation. However in order to fulfill better coding performance, the important changes in H.265/ MPEG-4 part 10 occur in the details of each functional element by including intra-picture prediction, a new 4x4 integer transform, multiple reference pictures, variable block sizes and a quarter pel precision for motion compensation, a daglocking filter, and improved entropy coding. Modifications have been made in the video coding layer of H.265 in order to achieve significant compression efficiency as compared to previous standards. The basic architecture of H.265 is shown in Figure1.

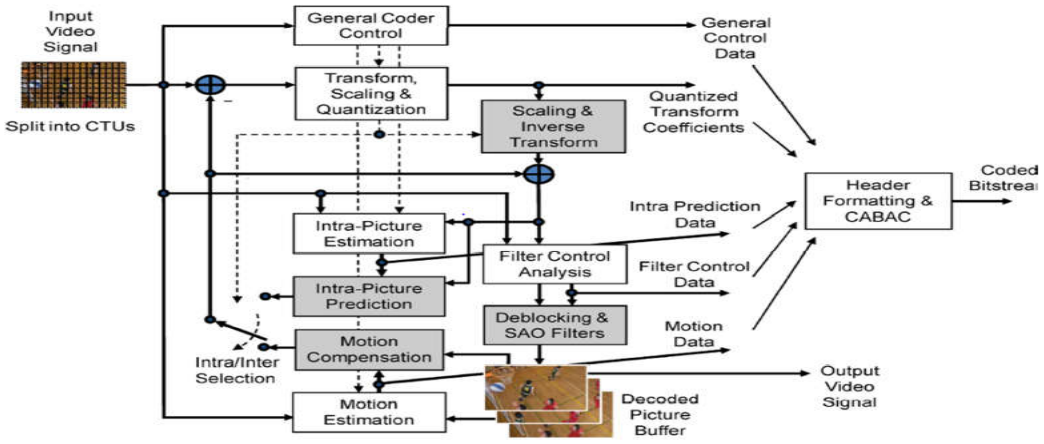

Figure 1: Block diagram of HEVC/H.265

In H.265, first the video source is divided into blocks of luma and chroma. Then the motion estimation and prediction are employed to exploit the temporal and spatial redundancies. Then transform coding, quantization and entropy coding are applied in serial, which finally generate the output bit stream. This bit stream can be used to transmit through networks or stored with optical or magnetic storage devices. The integer transform block, prediction block & scalar quantization blocks are explained in details section 2 & 3 in detail.

The decoding flow consists of a series of reversed operations in terms of the encoding process (Figure 2). The only operation added to the decoding flow is the loop-filter (deblocking filter). The purpose of this filter is to minimize the block distortions introduced by block based transformations and motion estimations.

The video decoding procedure is defined in existing standards (also for H.265), which means by imposing the decoding process with a collection of restrictions (such as the restrictions on bit stream and syntax), any encoding process that produces a decodable bit stream (decodable by the standard decoding process) is an applicable encoder. By this way, the developers have strong flexibility in developing the encoders in order to incorporate different applications with various requirements (such as compression quality, implementation cost, time to market, etc

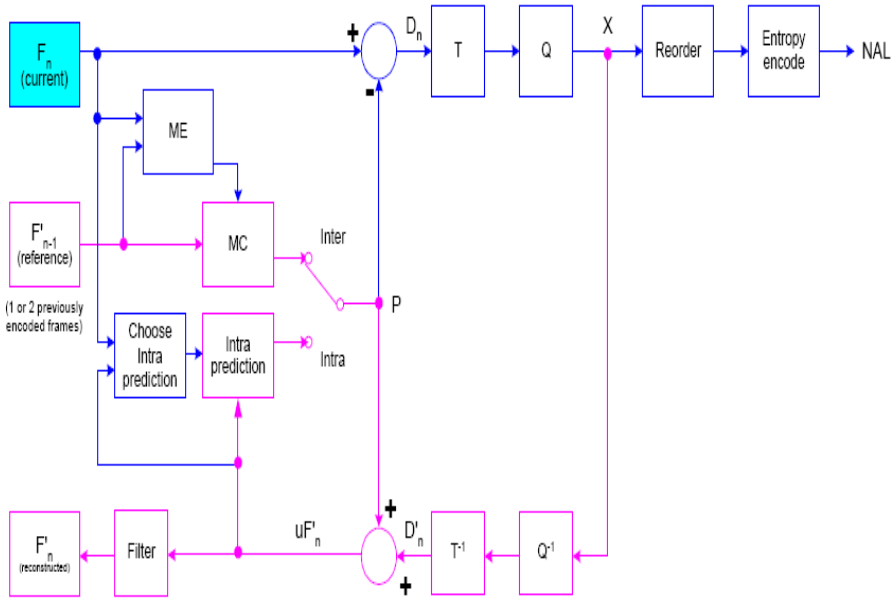

Figure 2 : Encoder block of HEVC/H.265

II. LITERATURE REVIEW

As in "[1]" focuses on one technical aspect that is key to the widespread adoption of digital video technology that is video compression. It gives us information about video formats and quality, video coding concepts. The concepts of H.264, its syntax, H.264 Prediction, H.264 transform and coding, and its performance can be clearly understood.

As in "[2]" focuses on Image and Video compression fundamentals, different Video coding standards like JPEG, MPEG, H.261, H.263, H.26L. Motion estimation and compensation, pre and post processing, rate, distortion and complexity concepts are discussed here. It also gives information about Video codec design and platforms to be used for Image and Video compression.

As in "[3]" paper focuses on Discrete Cosine Transform (DCT). Basically it gives us information of DCT"s part in video compression. It tells us about the DCT formulae to be used, properties of DCT. Comparisons of DCT with other image transforms like Karhunen-Loeve Transform (KLT) and Discrete Fourier Transform (DFT) is done here. Evaluation of DCT performance using a theoretic approach is carried out here.

As in "[4]" paper provides an overview of the technical features of H.264/AVC, describes profiles and applications for the standard, and outlines the history of the standardization process. The main goals of the H.264/AVC standardization effort have been enhanced compression performance and provision of a "network-friendly" video representation addressing "conversational" (video telephony) and "non conversational" (storage, broadcast, or streaming) applications.

As in "[5]"paper tells about Context-based adaptive variable-length coding (CAVLC) a new and important feature of the latest video coding standard, H.264/AVC. The direct VLSI implementation of CAVLC modified from the conventional run-length coding architecture will lead to low throughput and utilization. In this paper, an efficient CAVLC design is proposed.

As in "[6]" paper proposes the implementation of context adaptive variable length coder for H.264 video encoder. The implementation is capable of bringing about compression of video sequences as per user specification and is capable of processing high resolution pictures of sizes of up to 1024 x 768 pixels, encoding at a real time frame rate of 25 fps. The variable length coder has been realized using Verilog RTL coding. The compression achieved by the implementation is over 10 and the reconstructed picture quality is better than 35 dB.

As in "[7]" paper proposes a novel implementation of the core processors, the integer transform and quantization for H.264 video encoder using an FPGA. It is capable of processing the frames with the desired compression controlled by the user input. The algorithm and architecture of the components of the video encoder namely, integer transformation, quantization were developed, designed and coded in Verilog. It can process 1024x768 pixel color images in 4:2:0 formats at 25 frames per second. There constructed picture quality is better than 35 dB.

As in "[10]" paper epitomizes the précised methodology for power saving at all design levels for video decoding is proposed and enforced. Power intake is optimized at algorithm, architecture, circuit and physical levels by using the appropriate methods like parallelism, pipelining and memory access reduction. A new architecture of a low-power bit stream residual decoder for H.264/AVC baseline decoder. Low power building blocks are proposed and analyzed. Various power reduction techniques are utilized in the architecture level and the circuit level.

As in "[11]"paper exemplify the features of the new design provide approximately a 50% bit-rate savings for equivalent perceptual quality relative to the performance of prior standards (especially for a high-resolution video). In HEVC video coding standards single component improvement will not boost the performance of codec. i.e. enhancing the attainment in each block will makes the overall performance better.

As in "[12]"paper proponent the implementation and design of video single chip decoder for portable multimedia application. This chip has mixed hardware/software architecture to combine performance and flexibility. It has the low power consumption and highly flexibility.

As in "[13]" analyzed a VLSI implementation of CAVLC decoder for H.264/AVC and algorithm involved and design an efficient architecture. The architecture can decode event syntax in one cycle, and its maximum work frequency is 125MHz.Theseadvantages show that it can be used to implement video applications that require high throughput.

As in "[14]" analyzed Column-of-Pixel (CoP) memory arrangement to reuse the pixel between the de-blocking filter and the prediction unit. Further, they propose a hybrid scheduling to reduce the processing cycles and improve the system throughput. The main idea is that we use four pixel buffers to keep the Intermediate pixel value and perform the horizontal and vertical filtering process in one hybrid scheduling flow.

As in "[15]" depicts the present idea of pipelined SAD architecture for efficient SAD calculation. The proposed configuration is utilized in diamond search algorithm to carry out the motion estimation for assessing the performance of the design. The architecture proposed by the author employs the pipelining at 8×8 block, the overall design is implemented in TSMC 90nm technology and also operates at maximum frequency of 486MHz.

III. PROPOUND HEVC

It is possible to carry out the research work on uses of vedic mathematics algorithms over traditional methods that will provide effective throughput of processor. In this paper the main objective was around the speed and the future work can be done on power and area optimization.

IV. CONCLUSION

This paper presents the retention on different architecture algorithms of video CODEC H.265/HEVC using various techniques and comparison with previous video standards. The work done on different types of CODECs to boost the performance, especially in terms of speed are either based on pipelining, parallelisms, hazard free FSM and high speed multipliers, etc,. In the proposed HEVC Using vedic mathematics in different stages it is possible to reduce area, increase speed, decrease power consumption and to reduce the complexity of CODEC.

V. ACKNOWLEDGMENT

Our special gratitude to all who have supported towards enlargement of retention of HEVC.

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