

Operational Evaluation of Network on Chip Topologies

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Abstract- The Network on Chip (NoC) has developed as a substitute for wired or interconnection network for System on Chip (SoC). It acts as a way to reduce existing problems of interference, bandwidth desideratum, and potential and makes clock distribution work easier. The performance of the network can be evaluated by numerous factors but latency and throughput are primary characteristics of measurement. So, this paper contains study and evaluation of various existing topologies and their operational evaluation is done on the basis of latency and throughput.

I. INTRODUCTION

As the feature size decreases with time, the system performance was limited by interconnects. So, Network on Chip (NoC) evolved as an alternative to resolve interconnection problem, it gives sufficient bandwidth, promotes consecutive transmission, generates a stable structure and promotes more flexibility. The size of the chip has increased and there is a requirement for improvement due to hardware limitations [1] [2]. The 3-Dimension topology has come up as a way in which many silicon layers are put over the single chip, which produces improvement. Apart from this, 3-D connections decrease the number of wire utilized and on the other hand increase wire adaptability within the elements. It also makes the interface within technologies like DSP cores, MEMS, etc in which single IC is responsible for multiple tasks [3] [10].

In last few years, the 3-D topologies have increased chip design horizontally. This has also made the design more symmetric, stable, hence reducing noise and unwanted interference within numerous devices on the same board. Network on a chip developed as a better solution than traditional bus-based and point-to-point interconnection system and contain strength and ways to optimize complexity of current in multicore System on-chip communication[4][9].

Network topology provides a way to arrange nodes in a way so that various factors like delay, area utilized, and network cost, and throughput can be optimized. All these factors are useful in calculating the operational evaluation of system [5] [6]. This research paper contains the study, evaluation, and analysis of different network on chip topologies by comparing various parameters like injection rate, throughput with load offered.

II. PERFORMANCE EVALUATION MEASURABLE

A. Maximum end-to-end Latency

This is the time utilized by a packet till it is received. Latency is the total time utilized when the initial bit of the data packet is left from the data source until the end bit of data packet is acquired at the destination. Whereas, Maximum end-to-end latency is determined the maximal latency required to reach from source to destination at the extreme reach of a network. It is measured in terms of nanoseconds, microseconds, etc [13] [15] [14].

B. Dropping Probability

This is determined by the proportion of the data packet fall while traveling from source to destination at the time of transmission within the topology. [13] When dropping probability is 0, then it determines that data packet will never fall, and when it is 100, it is determined that all data packets will fell.

C. Throughput

This is the speed with which data packets are obtained at the destination point from Source point. It is quantified in terms of Mbps, Gbps, etc. It is influenced by metrics like routing strategy, flow control, simulation time, the packet received, packets sent, and packet length [13].

D. Hop Count

This is determined by the mean count of link and nodes from which a packet must go through at the time of transmission from source to destination. Average hop count is determined by the complete system [17].

E. Link Utilization

This is determined by the links deployed in the system. It is calculated from the number of transmission flits in each edge in unit time [17].

F. Path Diversity

This is determined when there are numerous minimum paths between the source and destination, and then it has large path diversity than the network which has a single route from source and destination. Adaptable load balanced traffic is provided by path diversity from the routes and give network strength to handle faulty nodes or routes within the system [17].

G. Hop Count

It is defined as the number of nodes a flit travel across while transferring from Source to Destination [17].

III. NETWORK ON CHIP (NOC) TOPOLOGIES

Topology is one of the primary factors which controls the performance of the network system [14]. So, in order to optimize the performance and functioning of the network for various needs and applications, different network on chip topologies have been developed. Here are some topologies which have been considered for operational evaluation:

A. Mesh Topology

It is one of the basic designs of Network on Chip architecture. There is a tie-in connection between all the nodes. This provides continual connection and multiple paths until the data packet reaches the destination from the source [8] [12]. Every node is in connection with four closest nodes. Due to higher hop count, the diameter of the mesh is also larger [16] [19].

Here is a figure representing 4X4 Mesh:

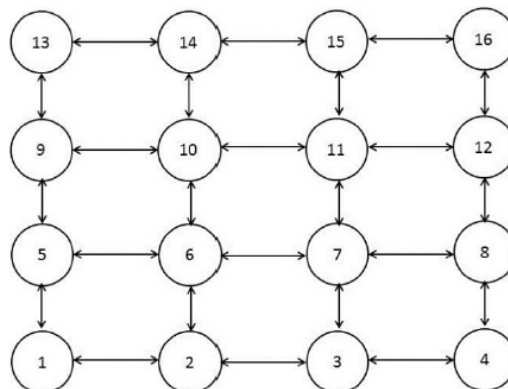


Fig. 1 4X4 Mesh

B. Diagonal Mesh Topology

It is similar to ordinary Mesh topology except for only one pair of the diagonal nodes is also connected to each other. Due to this similarity in architecture, the average diameter of both Mesh and Diagonal Mesh (DMesh) are same but average distance and bisection width vary [5].

Here, is a figure representing Diagonal Mesh (DMesh):

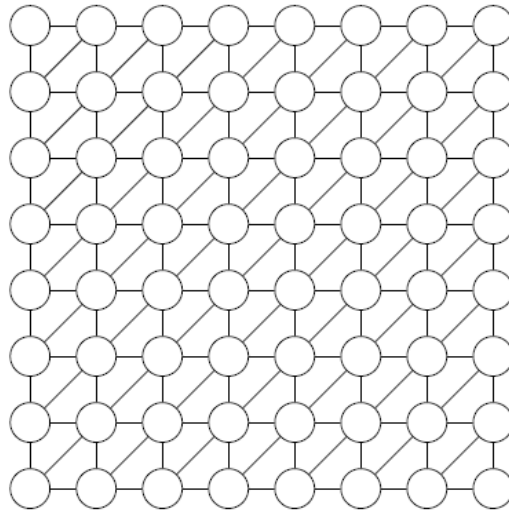


Fig. 2 DMesh

C. King Mesh

It is also developed from Mesh Topology. Whereas, in this, both the diagonal pairs are attached to each other. It is a Mesh-based network with maximum degree 8. The degree of this topology is 8. Nodes which are situated at the center of topology have a higher degree than the rest. The diameter of king mesh is less and lesser hop count [5].

Here, is a figure depicting King Mesh Network:

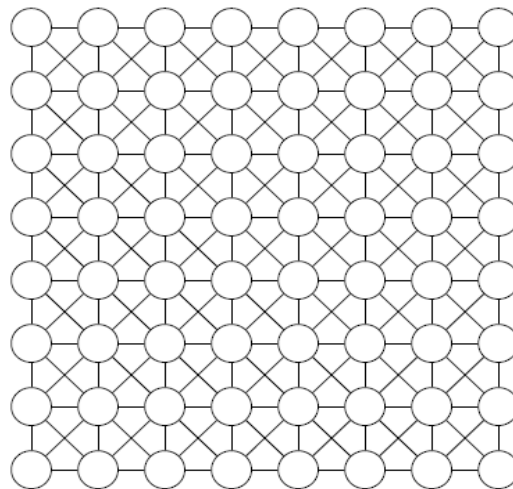


Fig. 3 King Mesh Topology

D. Torus Topology

The elementary design of this topology is Mesh structure. It contains wrap around edges alongside boundary nodes of same rows and columns [22]. This wrap around edges generates a structure with fewer diameters and less hop count. But, it requires larger wire length as compared to other topologies due to wrap around edges [7] [20].

Here, is a structure of Torus topology:

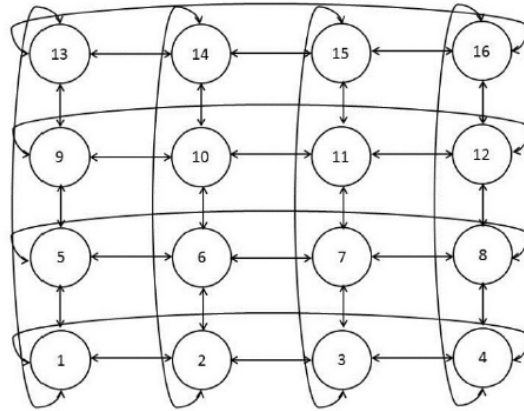


Fig. 4 Torus Topology

E. Cubic Ring Topology (CRing)

It is polymorphic topology in nature which means it will turn off resources dynamically by 30% and the average distance will increase by lesser than 5%. It has an easy, adaptable infra-structure, and on-demand bandwidth deciding structure for the network on chip communication. It is designed by eliminating specific network edges in a single dimension of a k-ary n-cube torus structure. This developed topology contains a graded allocation of Torus rings, various configurations, and normalized bandwidth. This allocation of rings joins two levels of hierarchy [7].

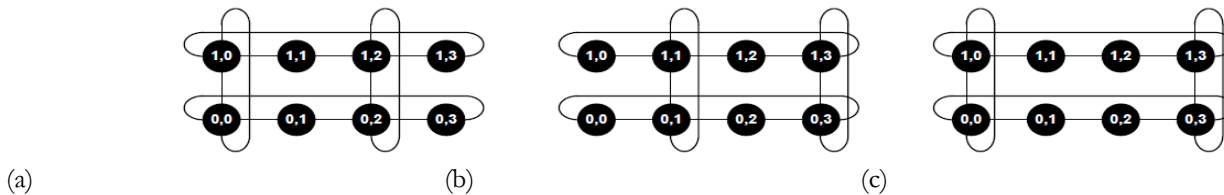


Fig. 5 An 8-node, 2,4-ary 2-cube R-ring c-ring network with (a) $R = \{1010,11\}$, (b) $R = \{0101,11\}$, and (c) $R = \{1001,11\}$

F. Concentrated Mesh with express channels (CMESH)

In this topology, a Mesh structure is decreased to a Radix-4 Mesh structure. This comes up with decreasing of average hop count and this reduces the component of zero load latency. This topology gives a good average completion time [11] [23].

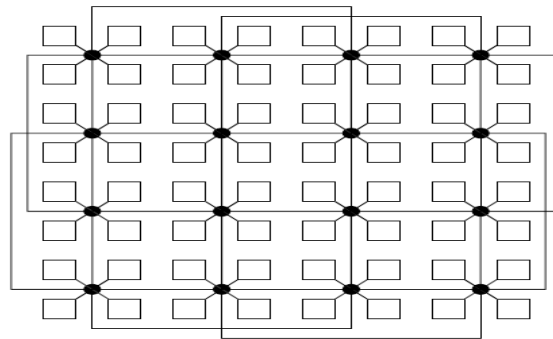


Fig. 6 CMesh Topology

G. Flattened Butterfly Network

It works best with high-radix routers. It is obtained by compressing the routers in every row of traditional butterfly topology but preserving same router connections. This topology resembles a generalized Hypercube [23], but if the focus is done on routers, this topology decreases the wiring complexity and hence increases scalability and efficiency [11].

IV. PERFORMANCE SIMULATION & ANALYSIS

Following is the graph representing the relation and comparison between various topologies studied above. The average latency and the offered load is taken into consideration below:

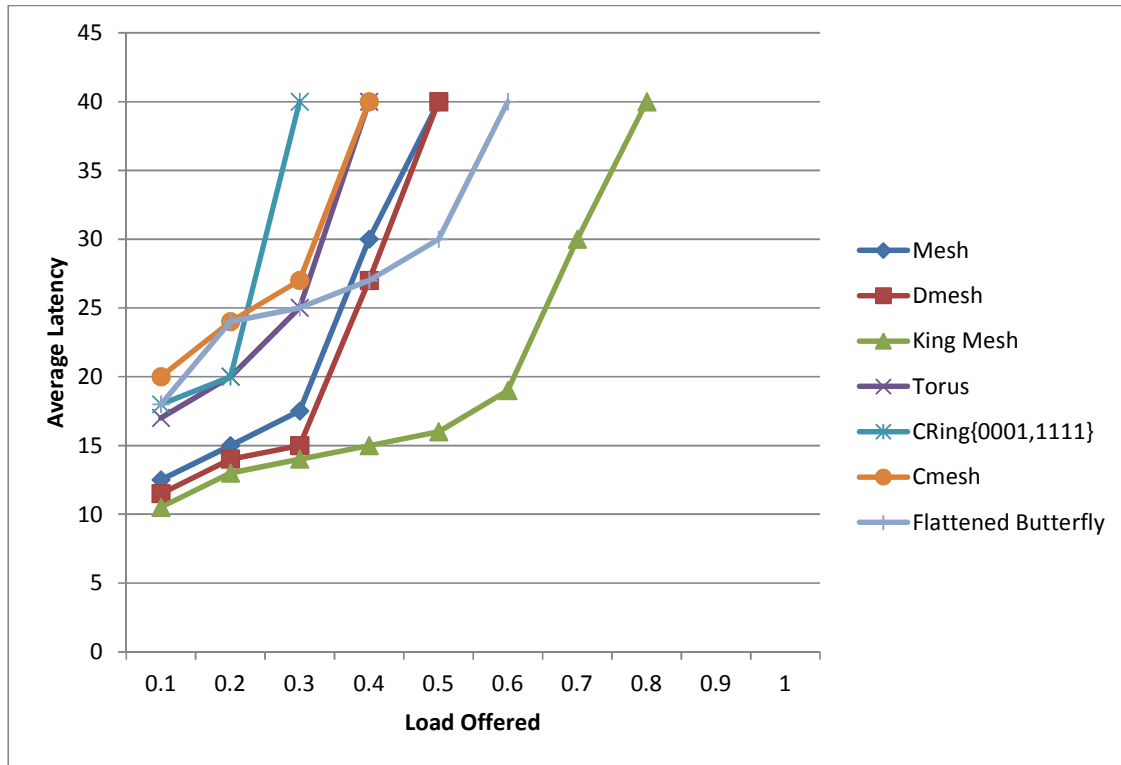


Fig. 7 Average Latency Vs Load Offered

V. CONCLUSION

The simulated results concluded that, when Average Latency is compared, King Mesh is better than DMesh topology, Mesh is better than Torus and Flattened Butterfly. Both DMesh and Mesh are leading Torus with a major amount of Latency. Cmesh is acquiring more latency than every other topology at every instant. Hence, making Cmesh a topology with maximum average latency. It has been observed that Latency increases extremely at a point and terminates simulation. It has been analyzed King Mesh is better in terms of Average Latency. It has a maximum number of edges which leads to a maximum degree. So, we have to maintain a tradeoff between degree and latency which requires more wires in order to reduce average latency.

In future work, we can decrease average degree with an objective to maintain latency.

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